Chettinad College of Engineering & Technology
Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai.

Department of Electronics and Communication Engineering

EC8453-Linear Integrated Circuits

Unit I - MCQ Bank

1. In practical application of current mirror, early voltage is assumed to be

A) Infinite

B) Zero

C) Unity

D) None Of The Mentioned

Answer: (A)

2. A Widlar Current Source Is Used

A) To Get Low Value Of Current

B) To Get High Value Of Cmrr

C) To Get Low Voltage Of Gain

D) To Get High Value Of Output

Answer: (A)

3. To Increase The Input Resistance In Differential Amplifier, Replace The Transistor By

A) Current Mirror

B) Current Repeater

C) Darlington Pair

D) All Of The Mentioned

Answer: (C)

4. To increase the input resistance, the differential amplifier replaces transistor by

A) Current Mirror

B) Current Repeater

C) Darlington Pair

D) All Of The Mentioned

Answer: (C)

5. In a network consisting of linear resistors and ideal voltage source, if the value of resistors are doubled, then voltage across each resistor _____

A) Increases Four Times

B) Remains Unchanged

C) Doubled

D) Halved

Answer: (B)

6. Which of the following is true about an ideal voltage source?

A) Zero Resistance

B) Small Emf

C) Large Emf

D) Infinite Resistance

Answer: (A)

7. If a current source is to be neglected, the terminals across the source are _____

A) Replaced By A Source Resistance

B) Open Circuited

C) Replaced By A Capacitor

D) Short Circuited

Answer: (B)

8. A Differential Amplifier amplifies

A) Input Signal With Higher Voltage

B) Input Voltage With Smaller Voltage

C) Sum Of The Input Voltage

D) None Of The Mentioned

Answer: (D)

9. A differential amplifier is capable of amplifying

A) DC Input Signal Only

B) AC Input Signal Only

C) AC & DC Input Signal

D) None Of The Mentioned

Answer: (C)

10. Find the correct match

Configuration	**Voltage gain and Input resistance**
1. Single Input Unbalanced Output	i. A_d = Rc/re , R_{i1} R_{i2} = $2\beta_{ac}RE$
2. Dual Input Balanced Output	ii. $A_{d= Rc/2re , Ri1}$ R_{i2} = $2\beta_{ac}RE$
3. Single Input Balanced Output	iii. A_d= Rc/re , R_i = $2\beta_{ac}RE$
4. Dual Input Unbalanced Output	iv. A_d = Rc/2re , R_i = $2\beta_{ac}RE$

A) 1-i , 2-iii, 3-iv, 4-ii
B) 1-iv, 2-ii, 3-iii, 4-i
C) 1-ii, 2-iv, 3-i , 4-iii
D) 1-iii, 2-i, 3-ii, 4-iv

Answer: (D)

11. Ideal op-amp has infinite voltage gain because

A) To Control The Output Voltage

B) To Obtain Finite Output Voltage

C) To Receive Zero Noise Output Voltage

D) None Of The Mentioned

Answer: (B)

12. Find the output voltage of an ideal op-amp. If V_1 and V_2 are the two input voltages

A) $V_O= V_1-V_2$

B) $V_O= A\times(V_1-V_2)$

C) $V_O = A\times(V_1+V_2)$

D) $V_O = V_1\times V_2$

Answer: (B)

13. Which factor determine the output voltage of an op-amp?

A) Positive Saturation

B) Negative Saturation

C) Both Positive And Negative Saturation Voltage

D) Supply Voltage

Answer: (C)

14. Open loop op-amp configuration has

A) Direct Network Between Output And Input Terminals

B) No Connection Between Output And Feedback Network

C) No Connection Between Input And Feedback Network

D) All Of The Mentioned

Answer: (A)

15. Find the output of inverting amplifier?

A) $V_o = Av_{in}$

B) $V_o = -Av_{in}$

C) $V_o = -A(V_{in1} - V_{in2})$

D) None Of The Mentioned

Answer: (B)

16. How to improve CMRR value

A) Increase Common Mode Gain

B) Decrease Common Mode Gain

C) Increase Differential Mode Gain

D) Decrease Differential Mode Gain

Answer: (B)

17. An inverting amplifier that amplifies dc input level is called

A) DC And AC Amplifier

B) AC Amplifier

C) DC Amplifier

D) None Of The Mentioned

Answer: (C)

18. When does the offset voltage compensating network must be used in inverting configuration?

A) When The Input Is Ac Voltage

B) When The Input Is Dc Voltage

C) When The Input Is Either AC Or DC Voltage

D) None Of The Mentioned

Answer: (B)

19. State the application in which summing, scaling or averaging amplifiers are used?

A) Multiplexers

B) Counters

C) Audio Mixers

D) All Of The Mentioned

Answer: (C)

20. How the value of output offset voltage is reduced in closed loop op-amp?

A) By Increasing Gain

B) By Reducing Gain

C) By Decreasing Bandwidth

D) By Reducing Bandwidth

Answer: (B)

21. How the slew rate is represented?

A) 1V/ms

B) 1V/s

C) 1V/μS

D) 1mv/s

Answer: (C)

22. Op-amps with wide bandwidth will have

A) Increase In Output

B) Higher Slew Rate

C) Low Response Time

D) None Of The Mentioned

Answer: (B)

23. To obtain a faster slew rate the op-amp should have

A) High Current And Large Compensating Capacitor

B) Small Compensating Capacitor

C) High Current Or Small Compensating Capacitor

D) Low Current Or Large Compensating Capacitor

Answer: (C)

24. In a high-frequency model of a JFET, which of these capacitances is present?

a: Gate-to-source capacitance

b: Gate-to-drain capacitance

c: Drain-to-source capacitance

A)a and b

B) a and c

C) b and c

D) a, b and c

Answer: (C)

25. Choose the incorrect statement for JFET(s).

A) Maximum Transconductance Occurs At $V_{gs}=0$

B) Transconductance Decreases Linearly With V_{gs}

C) Transconductance Increases Linearly With I_{ds}

D) Transconductance Does Not Depend On V_{ds}

Answer: (C)